What Is Claimed Is:

1. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions formed in the substrate and having a second conductivity type, with a channel region of the substrate defined therebetween;

an electrically conductive floating gate disposed over and insulated from at least a portion of the channel region, wherein the floating gate includes a horizontally oriented edge extending from a lateral side of the floating gate; and

an electrically conductive control gate having at least a portion thereof disposed laterally adjacent to and insulated from the horizontally oriented edge.

2. The device of claim 1, wherein a portion of the floating gate is disposed over and insulated from a portion of the first region.

3. The device of claim 1, further comprising:

a trench formed into a surface of the substrate, wherein the second region is formed underneath the trench, and wherein the channel region includes a first portion that extends generally along a sidewall of the trench and a second portion that extends generally along the surface of the substrate.

4. The device of claim 3, wherein the first and second portions of the channel region extend in directions that are generally perpendicular to each other.

5. The device of claim 3, wherein at least a portion of the control gate extends into the trench.

6. The device of claim 3, wherein:

the floating gate is generally elongated and extends in a direction generally parallel to the substrate surface; and

the control gate is generally elongated and extends in a direction generally perpendicular to the substrate surface.

7. The device of claim 1, further comprising:

a block of conductive material disposed over and in electrical contact with the first region.

8. The device of claim 7, wherein the floating gate is disposed laterally adjacent to and insulated from the block of conductive material.

9. The device of claim 1, wherein the floating gate is disposed generally over the entire second portion of the channel region.

10. The device of claim 1, wherein the floating gate edge is insulated from the control gate by insulating material having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

11. The device of claim 1, wherein the channel region first portion extends in a direction directly toward the floating gate.

12. The device of claim 7, further comprising:

a layer of insulating material disposed over the floating gate and laterally adjacent to the block of conductive material.

13. The device of claim 12, wherein the layer of insulating material is made of silicon nitride.

14. The device of claim 3, wherein the control gate includes:

a first portion extending along and insulated from a sidewall of the trench; and

a second portion extending along and insulated from a bottom wall of the trench.

15. The device of claim 14, wherein the control gate is generally "L" shaped.

16. The device of claim 14, wherein the control gate is generally rectangular shaped.

17. The device of claim 14, wherein the channel region includes a third portion that extends generally along the bottom wall of the trench.

18. The device of claim 17, wherein the channel region is generally "S" shaped.

19. The device of claim 1, further comprising:

a metal contact having a first portion disposed over and electrically connected to the second region and a second portion disposed over and insulated from the control gate.

20. The device of claim 7, wherein the block conductive material is a metal.

21. An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are generally parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a plurality of memory cells, each of the memory cells comprising:

first and second spaced-apart regions formed in the substrate having a second conductivity type, with a channel region of the substrate defined therebetween,

an electrically conductive floating gate disposed over and insulated from at least a portion of the channel region, wherein the floating gate includes a horizontally oriented edge extending from a lateral side of the floating gate, and

an electrically conductive control gate having at least a portion thereof disposed laterally adjacent to and insulated from the horizontally oriented edge.

22. The array of devices of claim 21, wherein for each of the memory cells, a portion of the floating gate is disposed over and insulated from a portion of the first region.

23. The array of devices of claim 21, further comprising:

a plurality of trenches formed into a surface of the substrate which are generally parallel to one another and extend across the isolation and active regions in a second direction that is generally perpendicular to the first direction, wherein each of the second regions is formed underneath one of the trenches.

24. The array of devices of claim 23, wherein for each of the memory cells, the channel region has a first portion extending generally along a sidewall of one the trenches and a second portion extending generally along the surface of the substrate.

25. The array of devices of claim 24, wherein for each of the memory cells, the first and second portions of the channel region extend in directions that are generally perpendicular to each other.

26. The array of devices of claim 24, wherein for each of the memory cells, at least a portion of the control gate extends into the trench.

27. The array of devices of claim 23, wherein for each of the memory cells:

the floating gate is generally elongated and extends in a direction generally parallel to the substrate surface; and

the control gate is generally elongated and extends in a direction generally perpendicular to the substrate surface.

28. The array of devices of claim 26, wherein for each active regions, each of the control gates therein extends across an adjacent isolation region and is electrically connected to one of the control gates disposed in another of the active regions.

29. The array of devices of claim 21, further comprising:

a plurality of blocks of conductive material each disposed over and in electrical contact with one of the first regions.

30. The array of devices of claim 29, wherein each of the floating gates are disposed laterally adjacent to and insulated from one of the blocks of conductive material.

31. The array of devices of claim 21, wherein each of the floating gates is disposed generally over the entire second portion of one of the channel regions.

32. The array of devices of claim 21, wherein each of the floating gate edges is insulated from one of the control gates by insulating material having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

33. The array of devices of claim 21, wherein each of the channel region first portions extends in a direction directly toward one of the floating gates.

34. The array of devices of claim 21, wherein the memory cells are formed as pairs of memory cells, and wherein each of the memory cell pairs share a single second region therebetween.

35. The array of devices of claim 21, wherein the memory cells are formed as pairs of memory cells, and wherein each of the memory cell pairs share a single first region therebetween.

36. The array of devices of claim 30, wherein each of the memory cells further comprises:

a layer of insulating material disposed over the floating gate and laterally adjacent to the block of conductive material.

37. The array of devices of claim 36, wherein the layer of insulating material is made of silicon nitride.

38. The array of devices of claim 24, wherein each of the control gates includes:

a first portion extending along and insulated from a sidewall of one of the trenches; and

a second portion extending along and insulated from a bottom wall of the one trench.

39. The array of devices of claim 38, wherein each of the control gates is generally "L" shaped.

40. The array of devices of claim 38, wherein each of the control gates is generally rectangular shaped.

41. The array of devices of claim 38, wherein each of the channel regions includes a third portion that extends generally along the bottom wall of the one trench.

42. The array of devices of claim 41, wherein each of the channel regions is generally "S" shaped.

43. The array of devices of claim 21, wherein each of the memory cells further comprises:

a metal contact having a first portion disposed over and electrically connected to the second region and a second portion disposed over and insulated from the control gate.

44. The array of devices of claim 29, wherein for each of the memory cells, the block conductive material is a metal.

45. A method of forming a semiconductor memory cell, comprising the steps of:

forming first and second spaced apart regions in a semiconductor substrate having a conductivity type different from that of the substrate, wherein a channel region of the substrate is defined between the first and second regions;

forming a floating gate of electrically conductive material disposed over and insulated from at least a portion of the channel region, wherein the floating gate includes a horizontally oriented edge extending from a lateral side of the floating gate; and

forming a control gate of electrically conductive material having at least a portion thereof disposed laterally adjacent to and insulated from the horizontally oriented edge.

46. The method of claim 45, wherein the floating gate is formed to be disposed over and insulated from a portion of the second region.

47. The method of claim 45, further comprising the step of:

forming a trench into a surface of the semiconductor substrate and spaced apart from the first region, wherein the second region is formed underneath the trench.

48. The method of claim 47, wherein the channel region includes a first portion that extends generally along a sidewall of the trench and a second portion that extends generally along the substrate surface.

49. The method of claim 48, wherein the first and second portions of the channel region extend in directions that are generally perpendicular to each other.

50. The method of claim 47, wherein at least a portion of the control gate is formed to extend into the trench.

51. The method of claim 47, wherein:

the floating gate is generally elongated and extends in a direction generally parallel to the substrate surface; and

the control gate is generally elongated and extends in a direction generally perpendicular to the substrate surface.

52. The method of claim 47, wherein the formation of the control gate includes forming a spacer of the electrically conductive material having a first portion extending along and insulated from a sidewall of the trench and a second portion disposed laterally adjacent to and insulated from the horizontally oriented edge.

53. The method of claim 45, further comprising the step of:

forming a block of conductive material disposed over and in electrical contact with the first region.

54. The method of claim 53, wherein the floating gate is disposed laterally adjacent to and insulated from the block of conductive material.

55. The method of claim 45, wherein the floating gate is formed generally over and insulated from the entire second portion of the channel region.

56. The method of claim 45, further comprising the step of:

forming a layer of insulating material between the floating gate edge and the control gate having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

57. The method of claim 45, wherein the channel region first portion extends in a direction directly toward the floating gate.

58. The method of claim 54, further comprising the step of:

forming a layer of insulating material disposed over the floating gate and laterally adjacent to the block of conductive material.

59. The method of claim 58, wherein the layer of insulating material is made of silicon nitride.

60. The method of claim 48, wherein the formation of the control gate includes the steps of:

forming a first portion of the control gate that extends along and is insulated from a sidewall of the trench; and

forming a second portion of the control gate that extends along and is insulated from a bottom wall of the trench.

61. The method of claim 60, wherein the control gate is generally "L" shaped.

62. The method of claim 60, wherein the control gate is generally rectangular shaped.

63. The method of claim 60, wherein the channel region includes a third portion that extends generally along the bottom wall of the trench.

64. The method of claim 63, wherein the channel region is generally "S" shaped.

65. The method of claim 45, further comprising the step of:

forming a metal contact having a first portion disposed over and electrically connected to the second region and a second portion disposed over and insulated from the control gate.

66. The method of claim 53, wherein the block conductive material is a metal.

67. A method of forming an array of semiconductor memory cells, comprising the steps of:

forming spaced apart isolation regions on the substrate having a first conductivity type which are generally parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

forming a plurality of spaced apart first and second regions in the semiconductor substrate having a second conductivity type, wherein a plurality of channel regions in the active regions of the substrate are defined each extending between one of the first regions and one of the second regions;

forming a plurality of floating gates of electrically conductive material each disposed over and insulated from at least a portion of one of the channel regions, wherein each of the floating gates includes a horizontally oriented edge extending from a lateral side of the floating gate; and

forming a plurality of electrically conductive control gates each having at least a portion thereof disposed laterally adjacent to and insulated from one of the horizontally oriented edges.

68. The method of claim 67, wherein the plurality of control gates are generally parallel to one another and extend in a second direction generally perpendicular to the first direction across the active and isolation regions.

69. The method of claim 67, wherein each of the floating gates are disposed over and insulated from a portion of one of the first regions.

70. The method of claim 67, further comprising the step of:

forming a plurality of trenches into a surface of the semiconductor substrate that are generally parallel to one another and extend in a second direction generally perpendicular to the first direction across the active and isolation regions, wherein each of the second regions is formed underneath one of the trenches.

71. The method of claim 70, wherein each of the channel regions includes a first portion that extends generally along a sidewall of one of the trenches and a second portion that extends generally along the substrate surface.

72. The method of claim 71, wherein the first and second portions of the channel region extend in directions that are generally perpendicular to each other.

73. The method of claim 71, wherein at least a portion of each of the control gates is formed to extend into one of the trenches.

74. The method of claim 71, wherein the formation of each of the control gates includes forming a spacer of the electrically conductive material having a first portion extending along and insulated from a sidewall of one of the trenches and a second portion disposed laterally adjacent to and insulated from one of the horizontally oriented edges.

75. The method of claim 70, wherein:

each of the floating gates is generally elongated and extends in a direction generally parallel to the substrate surface; and

each of the control gates is generally elongated and extends in a direction generally perpendicular to the substrate surface.

76. The method of claim 67, further comprising the step of:

forming a plurality of blocks of conductive material that are generally parallel to one another and extend in a second direction generally perpendicular to the first direction across the active and isolation regions, wherein each of the conductive material blocks is disposed over and in electrical contact with some of the first regions.

77. The method of claim 76, wherein each of the floating gates is disposed laterally adjacent to and insulated from one of the blocks of conductive material.

78. The method of claim 67, wherein each of the floating gates is formed generally over and insulated from the entire second portion of one of the channel regions.

79. The method of claim 67, further comprising the step of:

forming insulating material between each of the floating gate edges and the adjacent control gate having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

80. The method of claim 67, wherein each of the channel region first portions extends in a direction directly toward one of the floating gates.

81. The method of claim 77, further comprising the step of:

forming a layer of insulating material disposed over each of the floating gates and laterally adjacent to one of the blocks of conductive material.

82. The method of claim 81, wherein the layer of insulating material is made of silicon nitride.

83. The method of claim 71, wherein the formation of each of the control gates includes the steps of:

forming a first portion of the control gate that extends along and is insulated from a sidewall of one of the trenches; and

forming a second portion of the control gate that extends along and is insulated from a bottom wall of the one trench.

84. The method of claim 83, wherein each of the control gates is generally "L" shaped.

85. The method of claim 83, wherein each of the control gates is generally rectangular shaped.

86. The method of claim 83, wherein each of the channel regions includes a third portion that extends generally along the bottom wall of the one trench.

87. The method of claim 86, wherein each of the channel regions is generally "S" shaped.

88. The method of claim 67, further comprising the step of:

forming a plurality of metal contacts each having a first portion disposed over and electrically connected to one of the second regions and a second portion disposed over and insulated from one of the control gates.

89. The method of claim 76, wherein the block conductive material is a metal.

90. A method of operating an electrically programmable and erasable memory device having an electrically conductive floating gate disposed over and insulated from a substrate of semiconductor material, and an electrically conductive control gate having at least a portion

thereof disposed laterally adjacent to the floating gate and insulated therefrom by an insulating material, the method comprising the step of:

placing a voltage on the control gate that is sufficiently positive relative to a voltage of the floating gate to induce electrons on the floating gate to laterally tunnel from a horizontally oriented edge extending from a lateral side of the floating gate, through the insulating material, and onto the control gate via Fowler-Nordheim tunneling.

91. The method of claim 90, further comprising the steps of:

placing a positive voltage on a source region of the substrate formed at least partially underneath and insulated from the floating gate to capacitively couple the positive voltage onto the floating gate;

placing a positive voltage on a drain region of the substrate that is disposed underneath a trench formed in the surface of the substrate; and

placing a positive voltage on the control gate which has a first portion extending down into the trench and a second portion disposed laterally adjacent to the floating gate edge;

wherein electrons are induced to travel from the drain region, generally along a sidewall of the trench and onto the floating gate.

92. A method of operating an electrically programmable and erasable non-volatile memory cell having a first and a second state, and including an electrically conductive floating gate disposed over and insulated from a substrate of semiconductor material, and an electrically conductive control gate having at least a portion thereof disposed laterally adjacent to the floating gate, the method comprising the steps of:

establishing a first state of the memory cell by injecting electrons from a drain region of the substrate onto the floating gate, wherein the source region is disposed below a surface of the substrate and the injected electrons travel through the substrate in a direction generally perpendicular to the surface of the substrate; and

establishing a second state of the memory cell by removing electrons from the floating gate to the control gate via Fowler-Nordheim tunneling through an insulating material disposed

therebetween, wherein the removed electrons tunnel from a horizontally oriented edge extending from a lateral side of the floating gate, through the insulating material, and onto the control gate in a direction generally parallel to the surface of the substrate.

5